ABSTRACT

An architecture of hierarchical interconnect scheme for field programmable gate arrays (FPGAs). A first layer of routing network lines is used to provide connections amongst sets of block connectors where block connectors are used to provide connectability between logical cells and accessibility to the hierarchical routing network. A second layer of routing network lines provides connectability between different first layers of routing network lines. Additional layers of routing network lines are implemented to provide connectability between different prior layers of routing network lines. An additional routing layer is added when the number of cells is increased as the prior cell count in the array increases while the length of the routing lines and the number of routing lines also increases. Switching networks are used to provide connectability among same and different layers of routing network lines, each switching network composed primarily of program controlled passgates and, when needed, drivers.